HARDWARE
MANUAL FOR THE
MCXPCI/S
CARD

> **HARDWARE MANUAL FOR THE
> MCXPCI/S
> CARD**

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ANNEXES

I. THE MCXPCI/S

I.1 INTRODUCTION

You have just acquired an intelligent communications card from our MCXPCI range, and we thank you for your custom.

The cards in this range have been designed to be compatible with any machine fitted with a 5V PCI bus complying with the PCI 2.1 standard.

This documentation describes the hardware installation procedure and the technical specifications of the MCXPCI/S card.

This architecture is similar to that of a PC AT with a 486 microprocessor.
To manage the communications channels, it has their own microprocessor (AM486 DX5/P75 100 Mhz), 8 Mbytes of RAM which may be expanded up to 16 Mbytes, a hardware "watchdog", a keyboard controller and a 512 Kbyte FLASH EPROM containing a PC-compatible BIOS.

The MCXPCI/S is build from two boards :
       A MCXPCI/0 mother board
       A PCB/SERIAL extension board

I.2 THE VARIOUS OPERATING MODES

The card offers various operating modes that can be programmed via the group of mini-switches SW1-1 & SW1-2.

SW1-1	SW1-2	Operating mode
OFF	OFF	Built-In Firmware
ON	OFF	Stand Alone
OFF	ON	Reserved for ACKSYS use
ON	ON	MCXDOS

BUILT-IN FIRMWARE mode offers
- Access from the PC to the communications ports in asynchronous or synchronous mode without programming the card.
- A system for programming the FLASH EPROM in order to update the ACKSYS onboard firmware.
- A system for downloading client applications in MCS-86 format.

MCXDOS mode
This enables the development and operation of client applications onboard the card. DOS onboard applications can be loaded dynamically from the PC, but other applications require the use of a CompactFlash disk.

Stand Alone mode
Enables the card to execute applications onboard a CompactFlash disk autonomously, without intervention by the PC. This mode is typically used when the card is mounted in a RACK.

I.2.1 "Built-In Firmware" mode

The "Built-In Firmware" programming mode lets you operate the card from the PC using the ACKSYS firmware functions integrated into the flash EPROM of the card. ACKSYS supplies a device driver that runs on the host PC under the most familiar operating systems, giving your PC application an interface that complies with the PC's operating system and thus hides all the detailed PC / card dialogues that are implemented in firmware.

Two ACKSYS firmware versions are available:
- "Basic software" firmware, onboard all cards in the MCXPCI range as standard
- "Multiprotocol software" firmware, onboard the MCXPCI/570-2, MCXPCI/570-4, MCXPCI/570-8 and MCXPCI/570-F2 cards as standard, optionally on the MCXPCI/S and MCXPCI/BP-X cards, not available for the MCXPCI/U-X & MCXPCI/M128F-x1 cards

The following functions are provided by the **BASIC SOFTWARE FIRMWARE**:
- **Access to the communications ports in asynchronous mode,** limited to the MCXPCI/S and MCXPCI/BP-X cards
- **A system for programming the FLASH EPROM in order to update the firmware,** available on all cards in the MCXPCI range
- **A system for downloading files in MCS-86 format,** available on all cards in the MCXPCI range

The following functions are provided by the **MULTIPROTOCOL SOFTWARE FIRMWARE**:
- **Access to the communications ports in asynchronous and synchronous mode,** except on the MCXPCI/U-X & MCXPCI/M128F-x1 cards

Note that all these functions also depend on the ACKSYS device driver running on the host PC. In other words, it is advisable to consult the relevant documentation to find out what services are supported.

I.2.2 The MCXDOS mode

This mode enables the **development and operation of onboard applications** running under the operating system of your choice, provided that starting the application requires neither screen nor keyboard / mouse intervention.

DEVELOPING APPLICATIONS,
      IN THE DOS ENVIRONMENT ON THE CARD SIDE,
      IN THE DOS, WINDOWS 9X ENVIRONMENT ON THE PC SIDE,
requires the MCXDOS developer's kit.
Our development tools are still the standard tools on the market.
In the operational phase under these environments, the onboard application is loaded from the PC using the AUTOMCX software[1]. Note that the AUTOMCX software also exists for the Windows NT / 3.51 / 2000 operating system, so the card can also be operated in that PC environment.

DEVELOPING APPLICATIONS IN DIFFERENT ENVIRONMENTS requires the following equipment:
      A CompactFlash card for storing the operating system on the card side
      A keyboard connected to the card
      The MCXSPY software (VGA screen emulator in the text mode of the card on the PC)
The development tools are still the standard tools on the market.
This makes it possible, for example, to develop a QNX application in the card on a PC under Windows NT using the top performing development tools. Caution: the environment on the card side is restricted to non-graphical operating systems and the environment on the PC side is currently limited to DOS, Windows 95 / 98, Windows NT / 2000 & QNX.

I.2.3 The stand-alone mode

In this mode, the card starts up on the CompactFlash disk and then executes the onboard application. This is therefore an operating mode for the card, not a development operating mode.

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[1] Included in the MCXDOS kit

I.3 GUARANTEE

The guarantee period is laid down in our general terms of guarantee, i.e.:

A five-year guarantee on parts[1] and labour against any defect in manufacture or operation with the exception of faults caused by incorrect use or by the excessive action of a natural agent or circumstance.

Repairs under guarantee are carried out on our premises in an average of five working days.

CAUTION

♦ To ensure correct operation of the card, check that the battery is correctly connected.
♦ Electrical current from the mains supply, telephone and transmission cables may present a hazard.
  • Connect and disconnect the cables only when the machine in which your board is installed is unpowered.
  • Do not touch the cables during a storm.

<div style="text-align:center">

D A N G E R

</div>

<div style="text-align:center">

**NEVER JOIN OR SEPARATE THE CONNECTORS
WHILE THE MACHINE IS POWERED**

</div>

Faults are frequently caused by repeated handling of the SUB-D connectors while the machine is powered, which usually destroys the line amplifiers.

Most breakdowns are easily avoided if the above rule is obeyed.

<div style="text-align:center">

RESPECT IT!

</div>

---

[1] Except for the lithium battery, which is not guaranteed.

II. THE MCXPCI/0 MOTHER BOARD

The card must be installed on the machine in a 5V PCI socket complying with the PCI 2.1 standard or higher.

II.1 SYNOPSIS
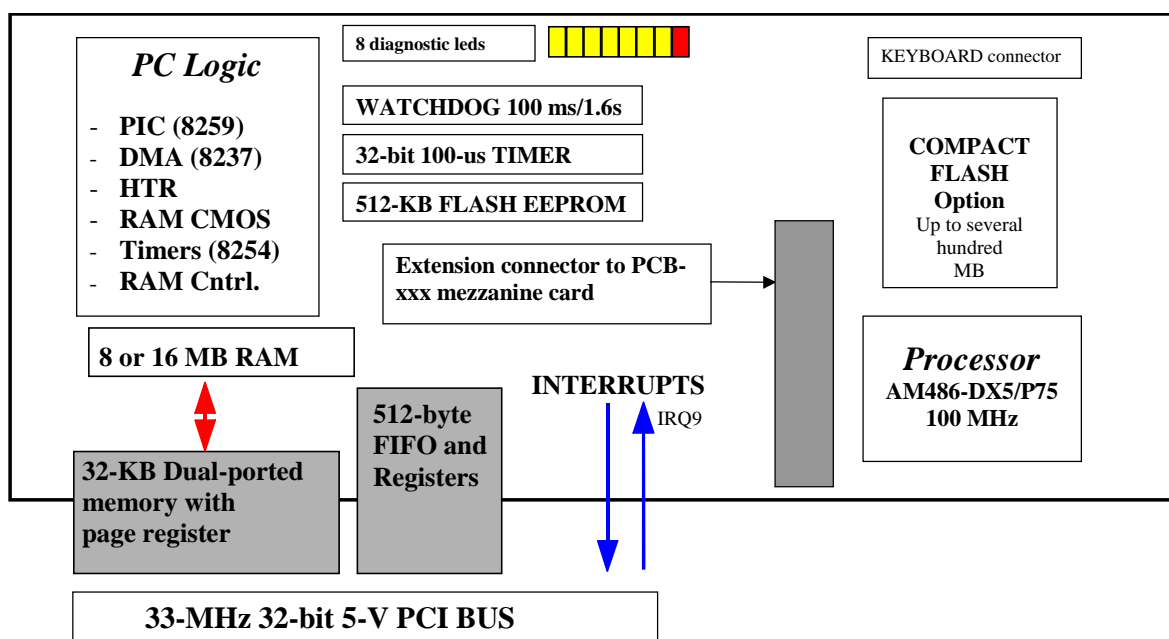
The hardware configuration of the card (the addresses of the double-port memory, the addresses of the I/O registers and the interrupt from the MCXPCI/0 card to the PC) is fixed by the PCI BIOS of the PC at the time the PC starts up. Caution: this configuration may change if you move the card to another PCI slot. Note that, with certain PCs, it is possible to specify the interrupt used by the card.

II.2 CONFIGURATION

SOLDER SIDE
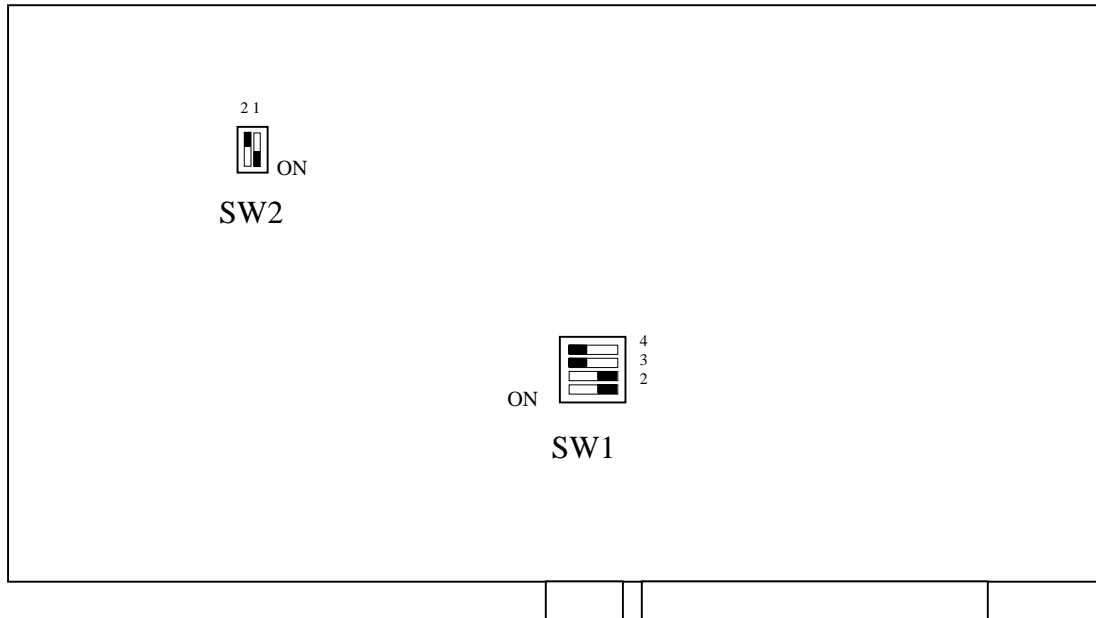
A silkscreen print on a plastic film attached to the board shows the configuration of each switch. The configuration on delivery is shown by the shading in the following tables.

SW1-1	SW1-2	Mode
OFF	**OFF**	**Built-In Firmware**
ON	OFF	Stand Alone
OFF	ON	Reserved for ACKSYS use
ON	ON	MCXDOS

SW1-3	Watchdog
ON	**Watchdog enabled**
OFF	Watchdog disabled

SW1-4	Action RESET PCI BUS
ON	**RESET MCXPCI**
OFF	No MCXPCI reset

SW1-4 lets you reset the MCXPCI/0 card when the PC's PCI bus is reset.

SW2-1	Battery
ON	**Battery Connected**
OFF	Battery Disconnected

SW2-2	Simulation of battery state (significant if SW2-1 OFF) or if battery dead
ON	Battery OK simulation
OFF	**Battery dead simulation**

Caution: Setting SW2-1 ON and SW2-2 ON is prohibited.

II.3 START-UP OF THE CARD

When power is applied, the MCXPCI card carries out a self-test, displaying the test currently being executed on a group of eight LEDs.

In the event of an error, the LEDs retain their state, thus enabling the cause of the error to be identified immediately.
The meanings of the various codes are as follows:

LED	0	1	2	3	4	5	6	7
	○	○	○	○	○	○	○	●
Bit	0	1	2	3	4	5	6	7

Code 01h .... Error register for CPU flags.
Code 02h .... CPU Error register.
Code 03h .... BIOS memory checksum error.
Code 04h .... DMA controller error.
Code 05h .... System TIMERS error.
Code 06h .... Error testing the address of 1st 64 K
or memory wrongly configured.
Code 07h .... Error testing the 1st 64 K RAM.
Code 08h .... INT controller error.
Code 09h .... INT detection unexpected.
Code 0Ah .... No TIMER interrupt.
Code 0Bh .... CPU already in protected mode.
Code 0Ch .... Error in DMA page register.
Code 0Dh .... No memory refresh.
Code 0Eh .... Error in keyboard controller.
Code 0Fh .... Cannot enter protected mode.
Code 10h .... Error in GDT or IDT registers.
Code 11h .... Error in LDT register.
Code 12h .... Error in task registry.
Code 13h .... Error in LSL instruction.
Code 14h .... Error in LAR instruction.
Code 15h .... Error in VERR / VERW.
Code 16h .... Error in address line A20.
Code 17h .... Unexpected exception.
Code 18h .... Shutdown during memory test.
Code 19h .... Copyright checksum error.
Code 1Ah .... Settings checksum error.
Code C0h .... Error in memory test.
Code C1h .... Error in IO/CHECK signal.
Code C2h .... "Watchdog time-out".
Code C4h .... "Bus time-out".

The following error codes are significant only in "Built-In Firmware" mode:

Code 81h .... Error in UART, SCC or SCA.
Code 82h .... Dual ported memory error.
Code 83h .... Unexpected TRAP error.
Code 84h .... Buffer memory error.
Code 85h .... Firmware checksum error.
Code 86h .... Lithium battery error.
Code 87h .... MCXPCI to PC interrupt error.
Code 88h .... "Watchdog" error.
Code 89h .... Error in FIFO access, flags or Interrupt on
                                                                 MCXPCI side or error reading FIFO
Code 8Bh .... SCC error during DMA high-speed test.
Code 8Ch .... General protection fault.
Code 8Dh .... Memory size error.
Code 8Eh .... NMI interrupt received.

In Built-In Firmware mode, if the self-test was correctly performed, LEDs 0 - 7 are lit and extinguished in succession, indicating that the card is now awaiting its starting code
  -    "RUN 01": basic software launched
  -    "RUN 02": Multiprotocol software launched

In MCXDOS mode, if the self-test was correctly performed, LEDs 0 - 7 are extinguished, indicating that the card is now awaiting its starting code
  -    "RUN 99": boot up in MCXDOS mode.
  -    "RUN 96": boot up from the CompactFlash disk.

In Stand-Alone mode, if the self-test was correctly performed, LEDs 0 - 7 are extinguished, and the card automatically starts from the CompactFlash disk.

If one of the errors mentioned above is encountered when power is applied to the card, you are advised to consult your reseller so that he can make all arrangements to repair the equipment as soon as possible.

III. THE PCB/SERIAL BOARD

The PCB-SERIAL extension includes all the communications logic

• a ZILOG 85C30 communications controller (or 85C230 in option)

• Line drivers required by the RS232D and RS422A standards.

This extension lets you add two asynchronous or synchronous RS232D or RS422A channels to the MCX-PCI/0 card, which then performs like one-quarter of an ACKSYS MCX-BP card.

COMPONENT SIDE   SOLDER SIDE
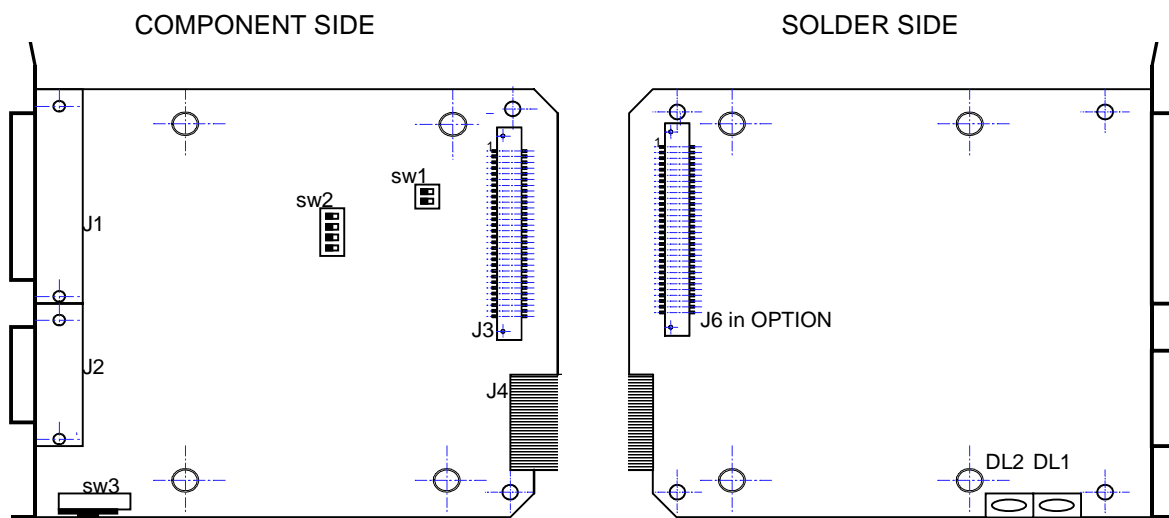
PCB/Serial extension

J1 connector : Sub-D 25 mâle connector, channel 1
J2 connector : Sub-D 9 mâle connector, channel 2
J3 connector : connector to associate the MCXPCI/0 & PCB-SERIAL extension.
J4 connector : channel 2 connector to plug the acksys converter cable (HE10-Sub-D25).
J6 connector : optional connector to connect a second PCB- extension.

SW1 switch : select IRQ # for INT SCC line
SW2 switch : select DMA # for DMA SCC line
SW3 switch : connect auxiliary +12V power available on J1 & J4 connectors

DL1 : LED lights if serial channel 1 in RS422, off in RS232
DL2 : LED lights if serial channel 2 in RS422, off in RS232

III.1 CONFIGURING THE EXTENSION

III.1.1 SW1 switch

SW1 defines the INT level used by the SCC communication controler (common to both serial channels).

SW1-1	IRQ3	ON = SCC	OFF = free
SW1-2	IRQ15	ON = SCC	OFF = free

III.1.2 SW2 switch

SW2 attributes a DMA channel to each SCC channel for both direction (Tx & Rx)

SW2-1	DRQ5	ON = Rx serial channel #2	OFF = free
SW2-2	DRQ3	ON = Tx serial channel #2	OFF = free
SW2-3	DRQ2	ON = Rx serial channel #1	OFF = free
SW2-4	DRQ1	ON = Tx serial channel #1	OFF = free

III.1.3 SW3 switch

The SW3 switch either enables or disables the presence of the +12V power supply on the J1 & J4 connectors/
In position VAUX-OFF, this voltage isn't avalaible.
In position VAUX-ON, this voltage is avalaible as described below :

J1 : pin #9
J4 : pin #17

III.1.4 Optional SUB D25 PIN Connector - channel 2

The channel 2 SUBD 9 pins connector can be replaced by a SUBD 25 pins connector, both of the card's channels have the same connections.
To do that, leave a free solt near the car and connect the conversion cable supplied by ACKSYS to J4 conenctor.

III.2 SIGNALS ON THE CONNECTORS

The PCB/SERIAL card offers 3 output connectors :

III.2.1 J1 connector and the optional SUBD 25 pin connector

These 25 pin male connectors are connected to lines 1 and 2 on the card.

**J1 SUB D25 PIN CONNECTOR - LINE 1 - and
OPTIONAL SUB D25 PIN CONNECTOR - LINE 2**

Pin #	Signal Direction	Description	CCITT V 24 Standard		Pin #	Signal Direction	Description	CCITT V 24 Standard
1	I	PGND	101		14	0	-TXCLOCK	
2	0	TXDATA	103		15	I	TXCLK-I	114
3	I	RXDATA	104		16	0	+TXCLOCK	
4	0	RTS	105		17	I	RXCLOCK	115
5	I	CTS	106		18	.	....	
6	.	....			19	I	-RXCLOCK	
7	I	GND 0V	102		20	0	DTR	108.2
8	I	CD	109		21	I	-RXDATA	
9[1]	0	+ 12 VDC (250 mA)			22	I	RI	125
10	0	....			23	I	+RXDATA	
11	I	+RXCLOCK			24	O	TXCLOCK	113
12	0	-TXDATA			25	.	....	
13	0	+TXDATA						

III.2.2 J2 Connector

This SUBD 9 pin male connector is attached to the second line.

J2 SUB D9 PIN CONNECTOR - LINE 2

Pin #	Signal Direction	Description
1	I	CD
2	I	RXDATA
3	O	TXDATA
4	O	DTR
5	I	GND 0V
6	.	....
7	O	RTS
8	I	CTS
9	I	RI

[1]Power available if the SW3 switch is in VAUX-ON position

III.2.3 J4 Connector

The J4 connector is provided (HE 10 26 pins) because it is not possible to output all the RS232 and RS422 signals on the J2 connector. You may directly attach a ribbon cable equipped with a standard SUB D25 pin connector to J4.

J4 HE 10 26 PIN CONNECTOR - LINE 2

Pin #	Signal Direction	Description	CCITT V 24 Standard	Pin #	Signal Direction	Description	CCITT V 24 Standard
1	I	PGND	101	14	O	DTR	108.2
2	O	-TXCLK		15	I	CD	109
3	O	TXDATA	103	16	I	-RXDATA	
4	I	TXCLK-I	114	17[2]	O	+ 12 VDC	
5	I	RXDATA	104	18	I	RI	125
6	O	+TXCLK		19	.	....	
7	O	RTS	105	20	I	+RXDATA	
8	I	RXCLK	115	21	I	+RXCLK	
9	I	CTS	106	22	O	TXCLK	113
10	.	....		23	O	-TXDATA	
11	.	....		24	.	....	
12	I	-RXCLK		25	O	+TXDATA	
13	I	GROUND 0V	102	26	.	....	

III.2.4 Electrical and mechanical specifications

POWER CONSUMPTION			DIMENSIONS	OPERATING CONDITIONS		
+ 5 V DC	+ 12 V DC	- 12 V DC	Length x Width	Relative humidity (non-condensing)	Temperature	Storage
1.5 A max / 7.5 W	110 mA max / 1320 mW	60 mA max / 720 mW		95% to +25°C	-5 to +65°C	-25 to +70°C

Max Power consumption calculations for + 5Vdc & +12 Vdc are based on :
  MCXPCI/S with 8 Mo RAM
  Both channels in RS422 at 500 Kbps
Max Power consumption calculations for - 12 Vdc are based on :
  MCXPCI/S with 8 Mo RAM
  Both channels in RS232 at 250 Kbps

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[2] Power available if the SW3 switch is in VAUX-ON position

INTERCALAIRE RECTO

INTERCALAIRE VERSO

APPENDIX

ANNEXE A   WRITING A DEVICE DRIVER

The information provided in this annexe tells a programmer all the points of entry into the card from the PC, i.e. the whole plan for addressing the card from the PC.

A.1   GENERAL

Dialogue between the card and the PC is ensured by the following mechanisms:

A 32-kilobyte dual ported memory enabling the bidirectional exchange of information between the PC and the card.

A card-to-PC interrupt.

A PC-to-card interrupt.

A 512-byte FIFO memory with write access on the card side, and read access on the PC side, constituting an alternative to the dual ported memory for the unidirectional exchange of information from the card to the PC.

A set of input / output registers that enable various operations:
  Read the FIFO
  Read FIFO status (empty, full, non-empty …)
  Read mode switch position (SW1-1 and SW1-2)
  Disable interrupt sent by the card
  Reset the card
  …

A.2   ADDRESSING THE DUAL PORTED MEMORY

The address of the 32-kilobyte dual ported memory, for example D00000h, is fixed by the PCI BIOS at the time the machine starts. This address can be read from the PCI configuration register called BAR1 (offset 14h).

This memory is in fact a page in the card's memory space, designated by a page number (see illustration below and paragraph A.3).
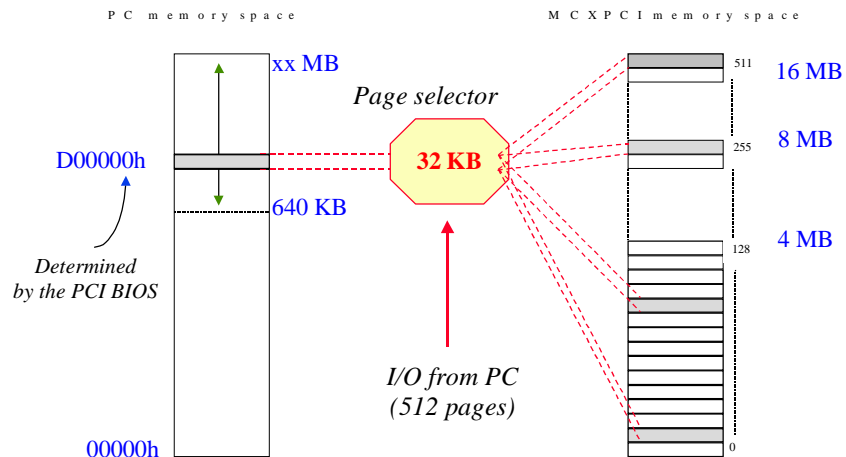
Address window	PAGE No.		Address Window	PAGE No.
0000 : 0000	00		8000 : 0000	10
0800 : 0000	01		8800 : 0000	11
1000 : 0000	02		9000 : 0000	12
1800 : 0000	03		9800 : 0000	13
2000 : 0000	04		A000 : 0000	14
2800 : 0000	05		A800 : 0000	15
3000 : 0000	06		B000 : 0000	16
3800 : 0000	07		B800 : 0000	17
4000 : 0000	08		C000 : 0000	18
4800 : 0000	09		C800 : 0000	19
5000 : 0000	0A		D000 : 0000	1A
5800 : 0000	0B		D800 : 0000	1B
6000 : 0000	0C		E000 : 0000	1C
6800 : 0000	D0		E800 : 0000	D1
7000 : 0000	0E		F000 : 0000	1E
7800 : 0000	0F		F800 : 0000	1F
			...	

The page number is designated by the board after the self-test phase (Page 1Ah) and can be changed by the PC (See paragraph A.3) or the card itself (See Annexe B).

The dual ported memory is addressed from the PC as standard memory without any restrictions, and all access modes are supported (8, 16 and 32 bits, aligned or otherwise).

A.3 ADDRESSING THE INPUT / OUTPUT REGISTERS

The base input / output address, e.g. C000h, is designated by the PCI BIOS at the time the machine starts up. This address can be read from the PCI configuration register called BAR0 (offset 10h).

Reading Base address + 0 – FIFO data register

D0 - D7 .... This register lets you read the contents of the FIFO, previously filled by the card (the FIFO has a capacity of 512 bytes). If the FIFO is empty, the value obtained is 0FFH (255).

Writing Base address + 0 – card reset

D0 - D7 .... Writing to this address causes an immediate reset of the card. The status of bits D0 - D7 is not significant

Write / Read Base address + 1 - write / read page no.

Bits D0 - D7 let you select / read a 32-kilobyte logical page in the card memory that will be accessible in the PC window.

D0 .... Logical page address - A15.

D1 .... Logical page address - A16.

D2 .... Logical page address - A17.

D3 .... Logical page address - A18.

D4 .... Logical page address - A19.

D5 .... Logical page address – A20.

D6 .... Logical page address – A21.

D7 .... Logical page address – A22.

Address bit A23 is defined by writing bit D0 at Base address + 5. Caution: the first write to this register disables the choice of page made by the card at the time it was initialized.

Write Base address + 2 - PC TO CARD Interrupt

D0 - D7 .... Writing to this register causes an interrupt on line IRQ9 of the card. As a way of waking the card, this is an alternative to the interrupt generated when writing to addresses 0 and 1 of the dual ported memory. The status of the data bits is not significant.

Write Base address + 3 - DISABLE CARD TO PC IRQ

D0 - D7 .... Writing to this register disables the interrupt generated by the card and sent to the PC. The status of the data bits is not significant.

Read Base address + 3 - FIFO STATUS

D0 .... MCX-TO-PC-INT bit

This bit indicates the status of the interrupt signal generated by the card to the PC.

0 : Interrupt disabled.

1 : Interrupt enabled.

D1 .... FIFO-EMPTY bit

0 indicates that the FIFO is empty, 1 indicates that the FIFO contains at least one byte.

D2 .... MCX-INT bit

1 indicates that the card has not yet disabled the interrupt generated by the PC.

D3 .... WIN-SET bit

0 indicates that the card has set its initial logical page and that the data read in the PC window are valid. 1 indicates that this operation has not yet been performed, or else the PC has selected a new logical page in the window.

D4 .... SW1-1 bit

1 indicates that the switch SW1-1 on the card is in the OFF position ; 0 indicates that it is in the ON position.

D5 .... SW1-2 bit

1 indicates that the switch SW1-2 on the card is in the OFF position ; 0 indicates that it is in the ON position

D6, D7 .... Non-significant

Read / Write Base address +5 – logical page bit A23

D0 .... This bit represents the address bit A23 of the 32-kilobyte logical page selected by the PC.

D1 - D7 .... Non-significant

Read / Write Base address +7 – Confirm card interrupt to PC

D0 .... This bit lets you authorize or prohibit the interrupt generated by the card to the PC.
D0 = 1   Interrupt authorized
D0 = 0   Interrupt prohibited

D1 - D7 .... Non-significant

A.4   CARD INTERRUPT TO PC

The interrupt used by the card in the PC, e.g. IRQ12, is determined by the PCI BIOS at the time the machine starts up. This interrupt can be read from the PCI configuration register called INTCFG (offset 3Ch).

This interrupt is generated by the card by writing to a register situated in the input / output addressing plan of the card. The PC can disable this interrupt by writing to the input / output register at the base address +3.

A.5   PC INTERRUPT TO CARD

The PC can generate an interrupt on line IRQ9 of the card:

by writing to the offsets 0 or 1 of the dual ported memory
by writing to the input / output port at the base address+2.

ANNEXE B PROGRAMMING THE CARD

This information is only intended to be used when writing programs internal to the card.
It tells the programmer the whole internal addressing plan specific to the card:

        Addresses of LEDs, watchdog, 100-us timer, interrupts, FIFO etc. (paragraph B.1)
        Addressing PCB-xxx mezzanine card (paragraph B.2)

All information about the PC logic unit is contained in the standard PC address plan and therefore is not provided in this Annexe.
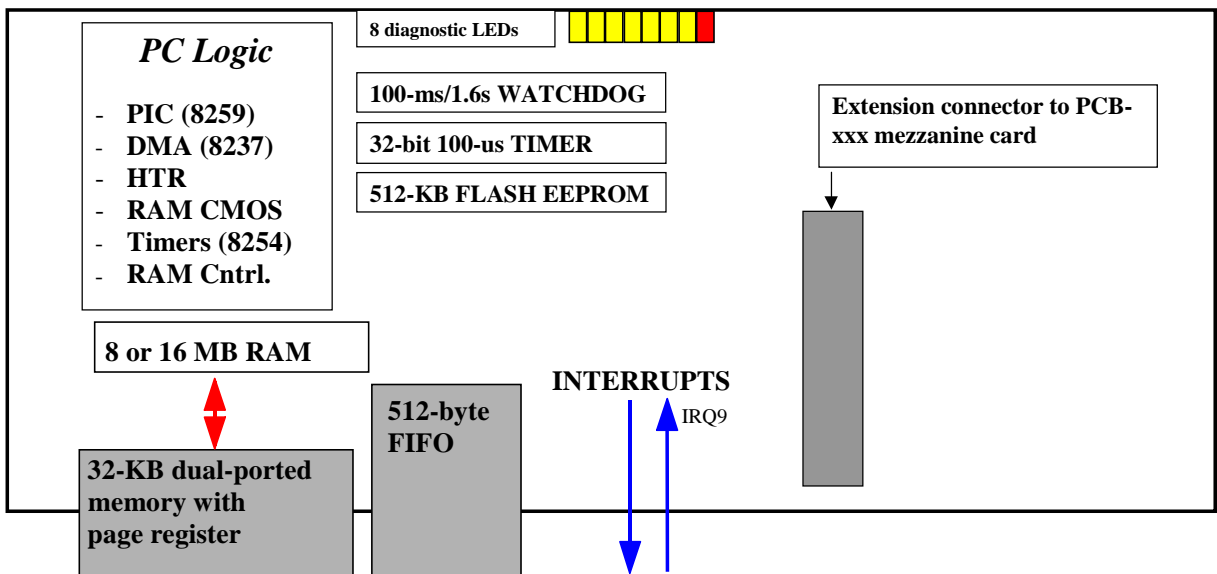
B.1   ADDRESSING THE GENERAL INPUT / OUTPUT REGISTERS

All the registers documented in this paragraph are **in the input / output addressing plan** internal to the MCXPCI/0 card. Caution: Most of the registers have different meanings for reading and writing.

* **Write address 80h - Display on the group of 8** LEDS

> D0 .... Status LED 0.
>
> D1 .... Status LED 1.
>
> D2 .... Status LED 2.
>
> D3 .... Status LED 3.
>
> D4 .... Status LED 4.
>
> D5 .... Status LED 5.
>
> D0   .... Status LED 6.
>
> D7 .... Status LED 7 (LED of different color)

Each bit at 1 corresponds to one LED illuminated.
Each bit at 0 corresponds to one LED extinguished.

* **Write address 500h - Enable interrupt to PC**

> D0 .... Interrupt line
>   1 = enabled
>   0 = disabled
>
> D1 - D7 .... Non-significant bits

* **Write / read address 501h – Programming FLASH memory**

> D0 .... Write FLASH enabled. This bit enables programming the FLASH memory containing the BIOS and the firmware.
>   0 = Write prohibited
>   1 = Write enabled
>
> D1 .... FLASH selection
>   0 = Upper 256 kilobytes
>   1 = Lower 256 kilobytes
>   After this bit has been modified, the card should be reinitialized.
>
> D2 - D7 .... Non-significant bits

* **Write address 503h - IRQ9 reset from PC.**

> D0 .... Reset interrupt generated by PC. The status of bit D0 is not significant. The interrupt generated by the PC is physically attached to the IRQ9 interrupt line of the card.
>
> D1 - D7 .... Non-significant bits

* **Write address 504h - Control register**

> D0 .... BAT-TEST bit
> If 0, permits reading the BAT-LOW bit (read bit D7 address 504h).
>
> D1 .... INT-MBX-ENABLE bit
> This bit enables the interrupts generated by the PC at the time of writing to address 0 or 1 of the dual ported memory. These interrupts are received on the IRQ9 line of the card. If set at 0, this bit prohibits this type of interrupt.
>
> D2 .... This bit controls the watchdog triggering time. The time is 1.6 seconds if D2 =1 and 100 ms if D2 =0
>
> D3 .... Initial address of the window (A15).
>
> D4 .... Initial address of the window (A16).
>
> D5 .... Initial address of the window (A17).
>
> D6 .... Initial address of the window (A18).
>
> D7 .... Initial address of the window (A19).
>
> Bits D3 - D7 permit definition of the initial 32-kilobyte logical page address seen by the PC. The other address bits, A20, A21, A22 and A23, are forced to 0 at the time of this operation. It should be noted that this logical page remains valid until the PC designates another one.

∗ **Read address 504h - Status register**

                 D0 .... FIFO Full bit
                                    This bit changes to 0 when the FIFO is full, thus prohibiting any new write to the FIFO. It also indicates the status of the IRQ10 interrupt line of the card.

                 D1 .... FIFO Empty bit
                                    This bit changes to 0 when the FIFO is empty. Reading the FIFO data register at address 510h when this bit is 0 returns the value FFh.

                 D2 .... FIFO Half Full bit
                                    This bit changes to 0 when the FIFO is half full.

                 D3 .... Indicates the status of the interrupt line to the PC.
                                      0 = Interrupt disabled
                                      1 = Interrupt enabled

                 D4 .... Indicates the position of the switch SW1-1
                                      0 = ON position
                                      1 = OFF position

                 D5 .... Indicates the position of the switch SW1-2
                                      0 = ON position
                                      1 = OFF position

                 D6 .... Always 1

                 D7 .... BAT-LOW bit
                                    0 indicates that the lithium battery must be replaced. Reading this bit is valid only if the BAT-TEST bit has been set to 0 (address 504h, bit of weight 0).

∗ **Write address 505h - Refresh "Watchdog"**

                 D0 - D7 .... Reset "Watchdog" to 0. The status of bits D0 - D7 is not significant.

∗ **Write address 506h - Control "Watchdog"**

> D0 .... Control "watchdog". The "watchdog" can again be disabled by the switch SW1-3; in the OFF position, the "watchdog" is disabled no matter what the content of the control register. In the ON position, by contrast, the "watchdog" is enabled and disabled as a function of the content of the control register.
>
>   0 = Watchdog disabled
>   1 = Watchdog enabled
>
> D1 - D7 .... Non-significant bits

∗ **Read address 507h - Read PAGE**

In read, bits D0 - D7 indicate the 32-kilobyte page number selected by the PC as dual ported memory.

> D0 .... Logical page address - A15.
>
> D1 .... Logical page address - A16.
>
> D2 .... Logical page address - A17.
>
> D3 .... Logical page address - A18.
>
> D4 .... Logical page address - A19.
>
> D5 .... Logical page address – A20.
>
> D6 .... Logical page address – A21.
>
> D7 .... Logical page address – A22.

Address bit A23 is defined by the status of bit D0 of the register at address 513h.

∗ **Write address 507h – FIFO data register**

      D0 - D7 .... 8-bit value to be written to FIFO

∗ **Write address 511h – 'Penalty' time-out**

      D0 - D7 .... Reserved for ACKSYS use. Register initialized by the card BIOS. Do not change this value.

∗ **Write address 512h – Confirm 0WS**

      D0 .... Confirm 0WS. If 0, this bit enables the I/O access mode without inserting a 'Wait State' for addresses above 500h.

      D1 - D7 .... Non-significant

∗ **Read address 513h – Logical page bit A23**

      D0 .... This is the most significant bit of the 32-kilobyte page number selected by the PC as dual ported memory. If 1, the selected logical page is beyond the 8th megabyte of the card memory. Note that only the PC can set this bit to 1 at Base address +5 and that a write on the card side at address 504h always sets this bit to 0.

      D1 - D7 .... Non-significant

∗ **Write address 514h – Card interrupt to PC**

      D0 .... If 1, this bit enables the card interrupt to PC. If set at 0, this bit prohibits this type of interrupt. Note that the PC can change this bit by writing to Base address+7.

      D1 - D7 .... Non-significant

∗ **Read addresses 516h - 519h and 51Ah– 32-bit 100-us counter**

      516h .... D0 – D7 of the counter

      517h .... D7 – D15 of the counter

      518h .... D16 - D23 of the counter

      519h .... D24 - D31 of the counter

Addresses 516h - 519h let you read the value of a 32-bit counter that is incremented every 100 µs. Initially read address 51Ah without noting its value, then read 516h, 517h, 518h and 519h in succession. This counter is reset to 0 after the card is reset.

B.2   ADDRESSING THE PCB/SERIAL REGISTERS

Please, notice the "SCC programmer's guide" is necessary to program the board.

The SCC base I/O space is fixed .at 0x600.
The SCC interrupt line is IRQ3 or IRQ5.

B.2.1 SCC addressing

           Base Address + 00h   Channel 2, command register - (Read/write)
           Base Address + 01h   Channel 2, data register - (Read/write)
           Base Address + 02h   Channel 1, command register - (Read/write)
           Base Address + 03h   Channel 1, data register - (Read/write)

B.2.2 General addressing

∗ **Base Address + 10h - Polling register (Read only):**

D0.......................... This bit provides the status of the SCC's interrupt line. It is set to 1 if the SCC interrupt line is active.
Bit D0 is set to zero after an SCC RESET.

D1,D2,D3,D4,D5 .. Not significant.

D6.......................... Status of the clock source:
- 1: SCC clock = 16 Mhz,
- 0: SCC clock = 14.7456 Mhz.

D7.......................... T/C Bit: Terminal Count (DMA)
If this bit is set to 1, it indicates that a DMA cycle has just completed for one of the unit's lines.
This bit is automatically reset to 0 if you read the address of the polling register + 1 (address 611h).
Warning: this register cannot be used to identify the DMA channel that just finished its cycle when several cycles finish at the same time; in that case, read the status registers of the various DMA controllers.
Finally, the "Terminal count" automatically generates an interrupt to the MCXPCI/0 card on the same line as the SCCs.

∗ **Base Address + 11h - Reset T/C bit (Read only):**

Reading this address zeroes the T/C bit (D7) that is read-latched to the polling register.

∗ **Base address + 12h - Read RING (Read only):**

This register lets you read the RING INDICATOR (RI) signal when the lines in question are operating in synchronous mode.

D0.......................... equals 1 if the RING signal is active on channel 1, 0 if not active.

D1.......................... equals 1 if the RING signal is active on channel 2, 0 if not active.

D2 to D7................ No significant

∗ **Base Address + 14h - RS232D/RS422A Configuration (Write only):**

The 2 least significant bits in this register let you configure each of the *Lite*-SERIAL extension's two channels in RS232D or RS422A mode.

D0.......................... Equals 1 if channel 1 is in RS422A; 0 if the channel is in RS232D.

D1.......................... Equals 1 if channel 2 is in RS422A; 0 if the channel is in RS232D.

D2 to D7................ No significant

∗ **Base Address + 15h - Clock source (Write only):**

This register controls the source of the SCC clock as described below:

> D0 to D6................ No significant
> D7......................... SCC clock source command:
>   0 = 16 Mhz,
>   1 = 14.7456 Mhz.

B.2.3 Interruptions and DMA

The SCC line interrupt is selected by SW1 switch. Three options are possible : IRQ3, IRQ15 or none. The default line is IRQ3.

The SCC DMA lines are activated by SW2 switch. Two DMA channels are necessary for each SCC serial channel, one for Tx transfer, other one for Rx transfer.
> SCC Channel 1 uses DRQ1 for Tx transfer and DRQ2 Rx transfer.
> SCC Channel 2 uses DRQ3 for Tx transfer and DRQ5 Rx transfer.

ANNEXE C   FEEDBACK SLIP

We need your comments and suggestions in order to improve the quality and ease of use of our documentation.

You can help us achieve this by completing this feedback slip and returning it to us.

Thank you in advance!

COMPANY:	
User:	
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Address:	

State clearly the version and serial number of the card, the software version and the version of the documentation you are commenting on:

MCXPCI/S	
EEPROM Revision	
Documentation Revision	

Please give marks from 0 to 10 to each of the following characteristics:

Format   ☐   Introduction   ☐   Organization   ☐

Clarity   ☐   Precision   ☐   Explanations   ☐

Errors :

If you find errors in this documentation, please either tell us the page number and the details, or amend the relevant pages and attach photocopies of them to this form.

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